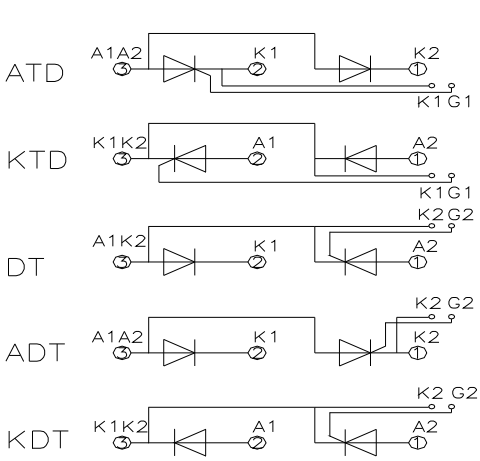
USR Semiconductor Co., Ltd

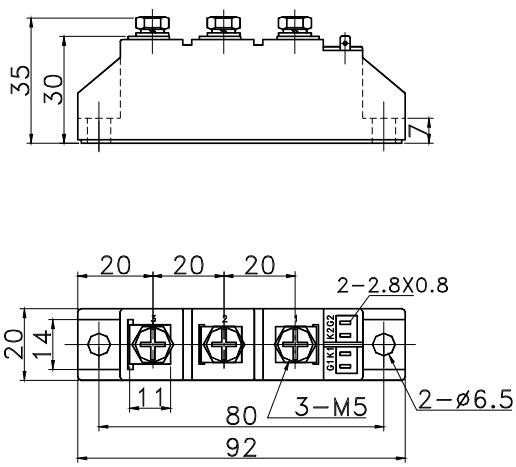
THYRISTOR/DIODE MODULE

TD55 ATD55 KT55 DT55 ADT55 KDT55

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T_j(°C)	VALUE			UNIT
				Min	Type	Max	
$I_{T(AV)}$ $I_{F(AV)}$	Mean on-state current	180° half sine wave 50Hz Single side cooled,T_C=85°C	125			55	A
$I_{T(RMS)}$	RMS on-state current	Single side cooled,T_C=85°C	125			86	A
V_{DRM} V_{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	V_{DRM}&V_{RRM} tp=10ms V_{DSM}&V_{RSM}= V_{DRM}&V_{RRM}+200V respectively	125	600		1800	V
I_{DRM} I_{RRM}	Repetitive peak current	at V_{DRM} at V_{RRM}	125			8	mA
I_{TSM}	Surge on-state current	10ms half sine wave V_R=60%V_{RRM}	125			1.25	KA
I^2t	I^2T for fusing coordination					7.90	A^2s*10^3
V_{TO}	Threshold voltage		125			0.85	V
r_T	On-state slop resistance					3.47	mΩ
V_{TM}	Peak on-state voltage	I_{TM}=165A	125			1.50	V
dv/dt	Critical rate of rise of off-state voltage	V_{DM}=67%V_{DRM}	125			800	V/μs
di/dt	Critical rate of rise of on-state current	From 67%V_{DRM} to 165A, Gate source 1.5A t_r ≤0.5μs Repetitive	125			50	A/μs
I_{GT}	Gate trigger current	V_A=12V, I_A=1A	25	30		100	mA
V_{GT}	Gate trigger voltage			0.8		2.0	V
I_H	Holding current			20		100	mA
V_{GD}	Non-trigger gate voltage	At 67%V_{DRM}	125			0.2	V
$R_{th(j-c)}$	Thermal resistance Junction to heatsink	At 180^0 sine' Single side cooled				0.530	°C /W
V_{iso}	Isolation voltage	50Hz,R.M.S,t=1min,I_{iso}:1mA(MAX)		2500			V
F_m	Thermal connection torque(M5)				0.20		N·m
	Mounting torque(M6)				0.30		N·m
T_{stg}	Stored temperature			-40		140	°C
W_t	Weight				100		g
Outline	201F3						

OUTLINE DRAWING & CIRCUIT DIAGRAM





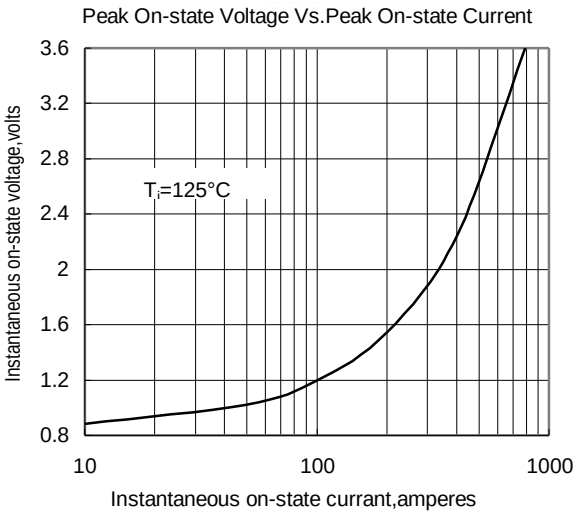


Fig.1

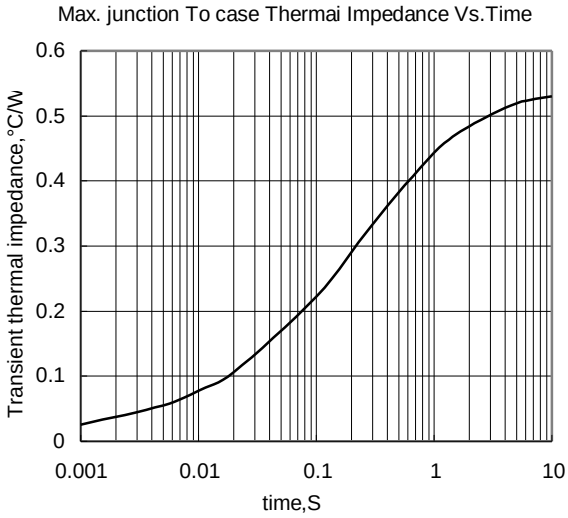


Fig.2

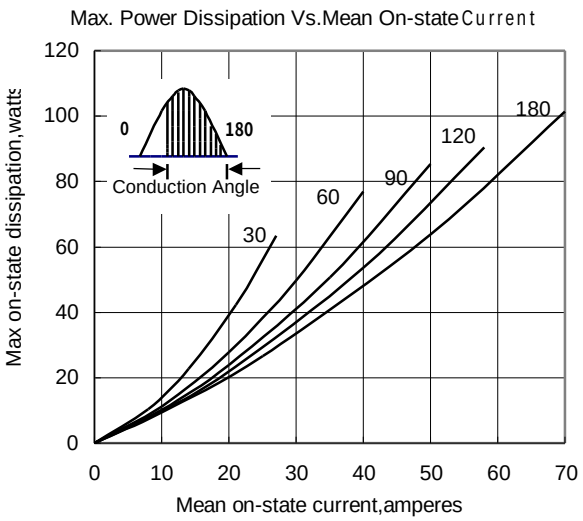


Fig.3

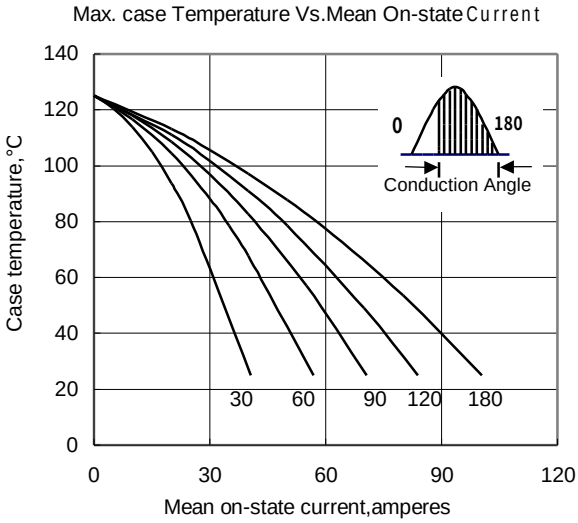


Fig.4

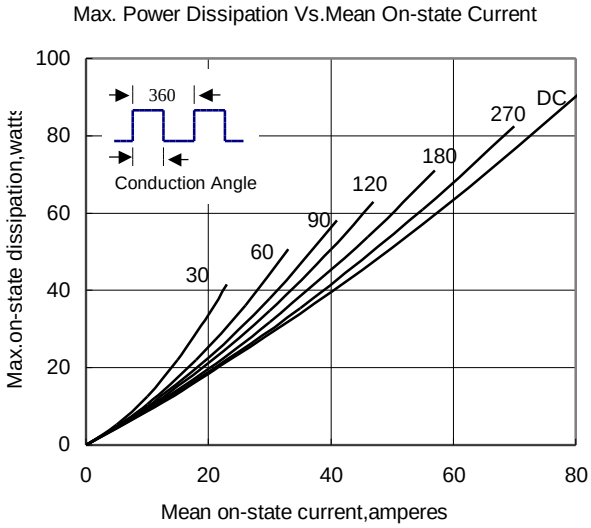


Fig.5

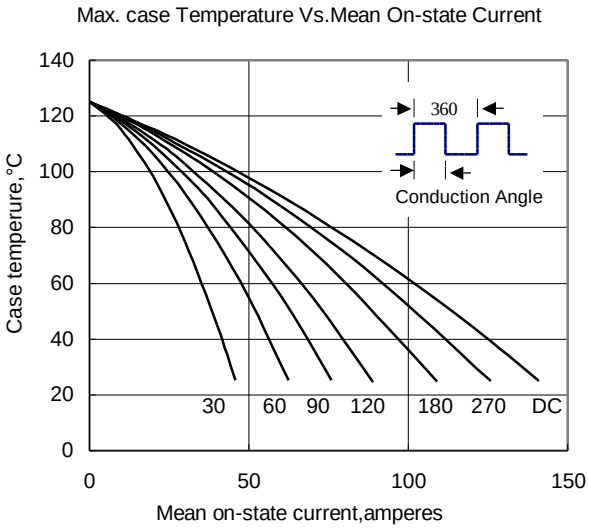


Fig.6

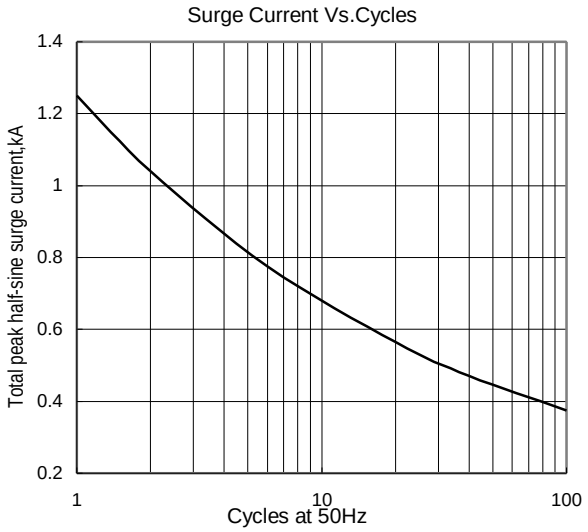


Fig.7

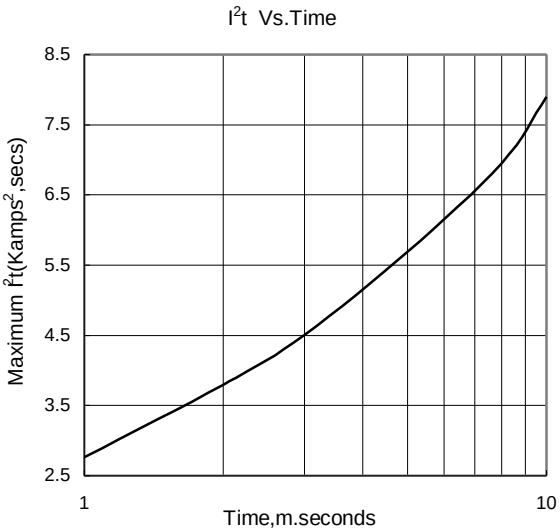


Fig.8

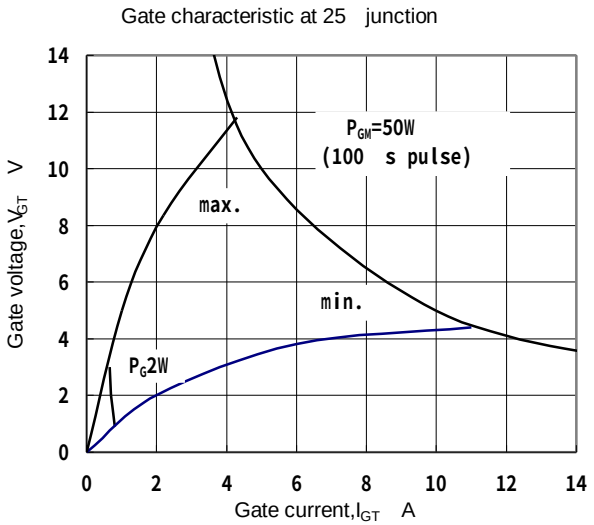


Fig.9

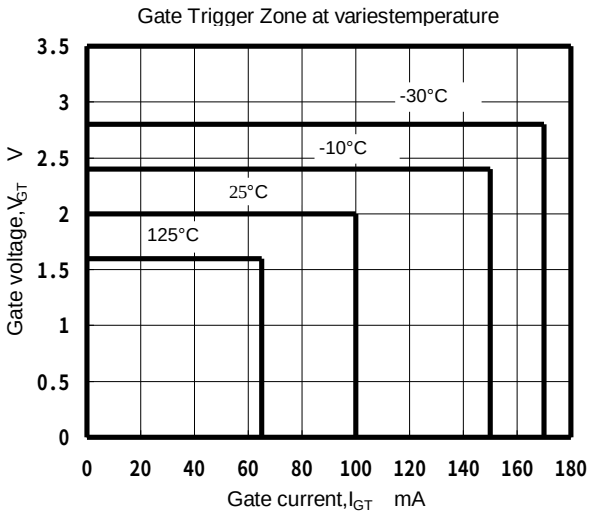


Fig.10