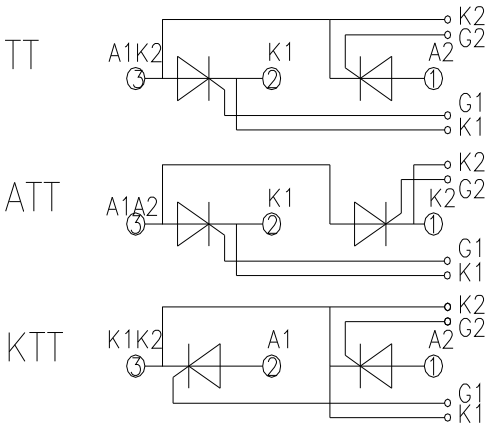
# USR Semiconductor Co., Ltd

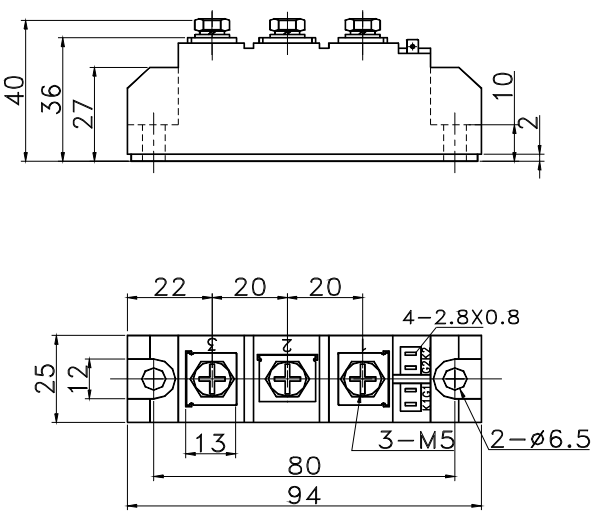
THYRISTOR MODULE

**TT110 ATT110 KTT110**

| SYMBOL | CHARACTERISTIC | TEST CONDITIONS | $T_j$(°C) | VALUE | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Type | Max | |
| $I_{T(AV)}$ | Mean on-state current | 180° half sine wave 50Hz<br>Single side cooled,$T_C$=85°C | 125 | | | 110 | A |
| $I_{T(RMS)}$ | RMS on-state current | as AC switch | | | | 225 | A |
| $V_{DRM}$<br>$V_{RRM}$ | Repetitive peak off-state voltage<br>Repetitive peak reverse voltage | $V_{DRM}$&$V_{RRM}$ tp=10ms<br>$V_{DSM}$&$V_{RSM}$= $V_{DRM}$&$V_{RRM}$+200V respectively | 125 | 600 | | 1600 | V |
| $I_{DRM}$<br>$I_{RRM}$ | Repetitive peak current | at $V_{DRM}$<br>at $V_{RRM}$ | 125 | | | 12 | mA |
| $I_{TSM}$ | Surge on-state current | 10ms half sine wave<br>$V_R$=60%$V_{RRM}$ | 125 | | | 2.40 | KA |
| $I^2t$ | $I^2T$ for fusing coordination | | | | | 29.3 | $A^2s*10^3$ |
| $V_{TO}$ | Threshold voltage | | 125 | | | 0.8 | V |
| $r_T$ | On-state slop resistance | | | | | 2.29 | mΩ |
| $V_{TM}$ | Peak on-state voltage | $I_{TM}$=330A | 125 | | | 1.69 | V |
| dv/dt | Critical rate of rise of off-state voltage | $V_{DM}$=67%$V_{DRM}$ | 125 | | | 800 | V/μs |
| di/dt | Critical rate of rise of on-state current | From 67%$V_{DRM}$<br>to 330A, Gate source 1.5A<br>$t_r$ ≤0.5μs Repetitive | 125 | | | 100 | A/μs |
| $I_{GT}$ | Gate trigger current | $V_A$=12V, $I_A$=1A | 25 | 30 | | 100 | mA |
| $V_{GT}$ | Gate trigger voltage | | | 1.0 | | 2.0 | V |
| $I_H$ | Holding current | | | 20 | | 100 | mA |
| $V_{GD}$ | Non-trigger gate voltage | At 67%$V_{DRM}$ | 125 | | | 0.2 | V |
| $R_{th(j-c)}$ | Thermal resistance<br>Junction to heatsink | At $180^0$ sine' Single side cooled | | | | 0.250 | °C /W |
| $V_{iso}$ | Isolation voltage | 50Hz,R.M.S,t=1min,$I_{iso}$:1mA(MAX) | | 2500 | | | V |
| $F_m$ | Thermal connection torque(M5) | | | | 0.2 | | N·m |
| | Mounting torque(M6) | | | | 0.3 | | N·m |
| $T_{stg}$ | Stored temperature | | | -40 | | 140 | °C |
| $W_t$ | Weight | | | | 160 | | g |
| Outline | 202F3 | | | | | | |

**OUTLINE DRAWING & CIRCUIT DIAGRAM**



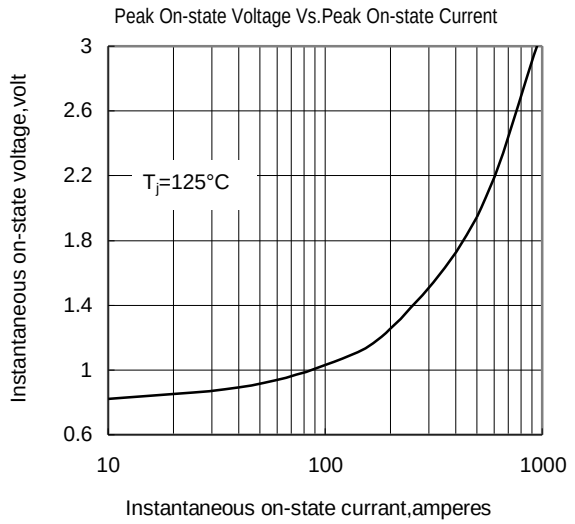



Fig.1

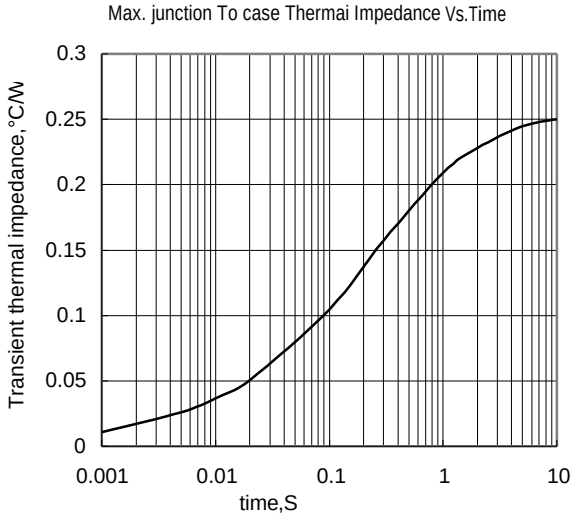



Fig.2

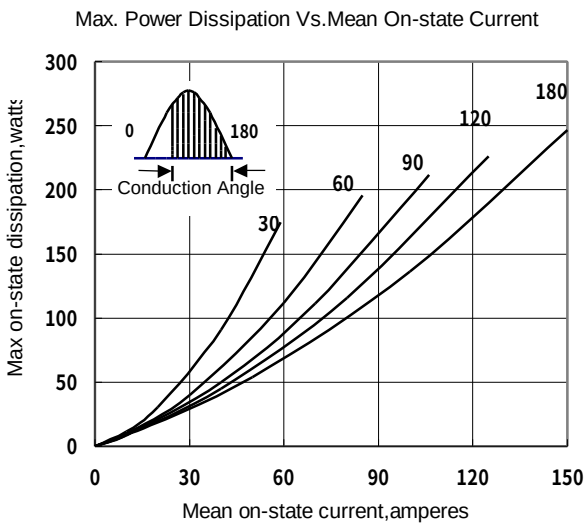



Fig.3

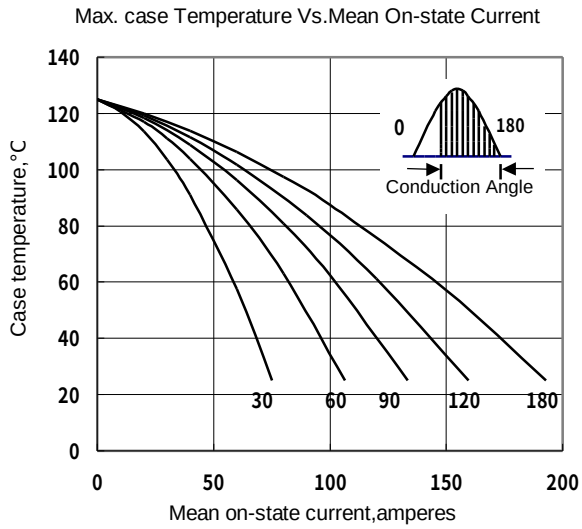



Fig.4

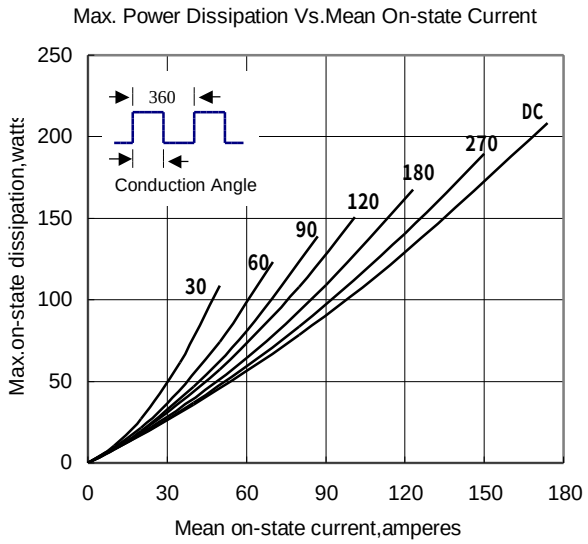



Fig.5

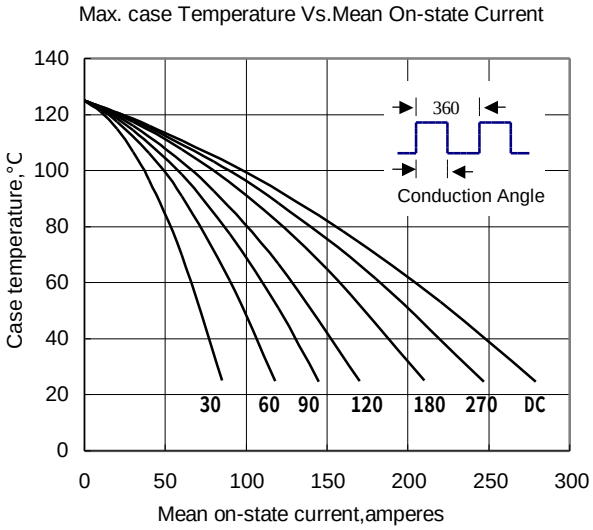



Fig.6

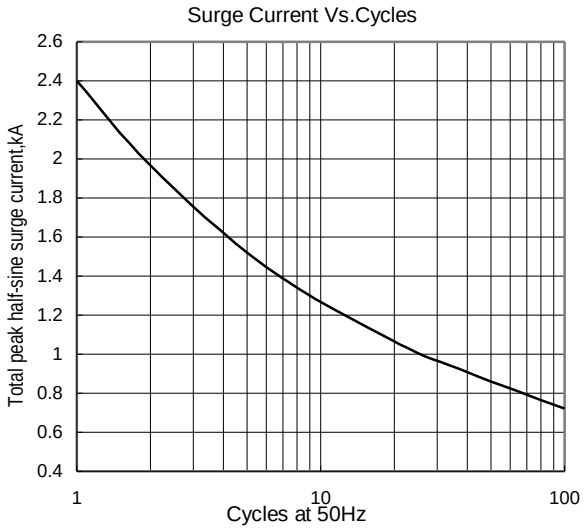



Fig.7

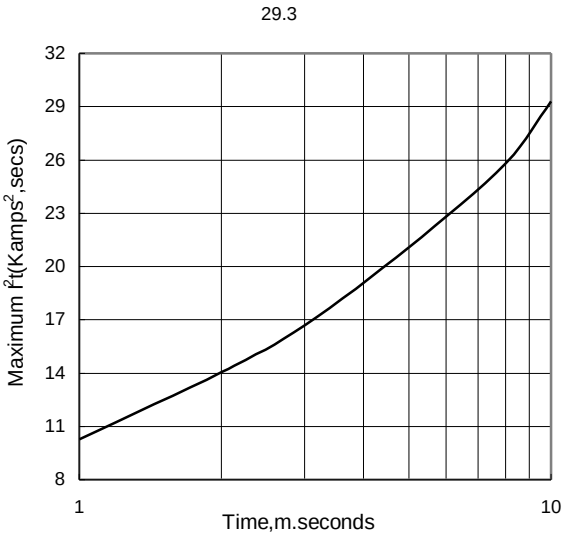



Fig.8

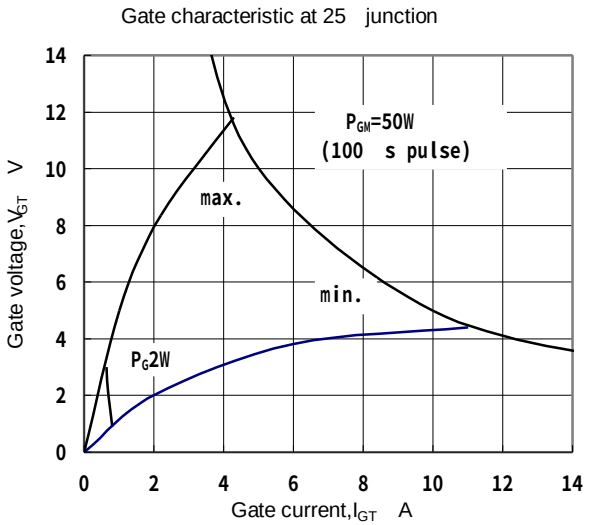



Fig.9

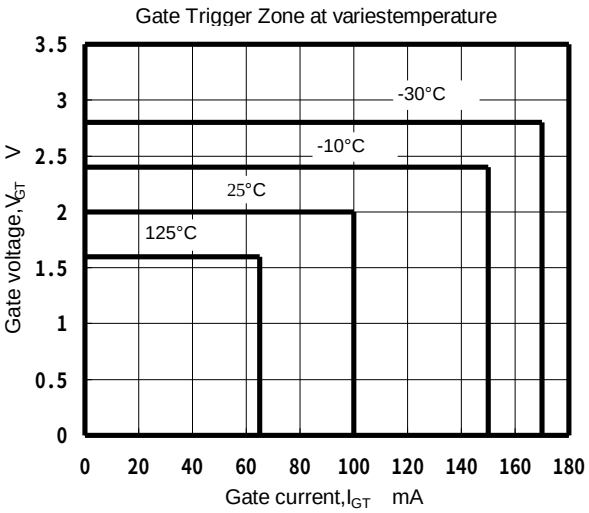



Fig.10