

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T _j (°C)	VALUE			UNIT
				Min	Type	Max	
I _{T(AV)}	Mean on-state current	180° half sine wave 50Hz Double side cooled, T _{HS} =55°C	115			1040	A
I _{T(AV)}	Mean on-state current	180° half sine wave 50Hz Double side cooled, T _{HS} =80°C	115			688	A
V _{DRM} V _{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	V _{DRM} &V _{RRM} tp=10ms V _{DSM} &V _{RSM} = V _{DRM} &V _{RRM} +100V respectively	115	800		1800	V
I _{DRM} I _{RRM}	Repetitive peak current	at V _{DRM} at V _{RRM}	115			80	mA
I _{TSM}	Surge on-state current	10ms half sine wave	115			12	KA
I ² T	I ² T for fusing coordination	V _R =0.6V _{RRM}				720	A ² s*10 ⁻³
V _{TO}	Threshold voltage		115			1.56	V
r _T	On-state slop resistance					0.33	mΩ
V _{TM}	Peak on-state voltage	I _{TM} =3000A, F=24KN	115			2.55	V
dv/dt	Critical rate of rise of off-state voltage	V _{DM} =0.67V _{DRM}	115			500	V/μs
di/dt	Critical rate of rise of on-state current	From 67%V _{DRM} to 1000A, Gate source 1.5A t _r ≤0.5μs Repetitive	115			600	A/μs
I _{rm}	Reverse recovery current	I _{TM} =800A, tp=1000μs, di/dt=-40A/μs, V _R =50V	115		100		A
t _{rr}	Reverse recovery time				5.8		μs
Q _{rr}	Recovery charge				290	320	μC
t _q	Circuit commutated turn-off time	I _{TM} =800A, tp=1000μs, V _R =50V dv/dt=30V/μs, di/dt=-40A/μs	115	15		35	
I _{GT}	Gate trigger current	V _A =12V, I _A =1A	25	40		300	mA
V _{GT}	Gate trigger voltage			0.9		3.0	V
I _H	Holding current			20		500	mA
V _{GD}	Non-trigger gate voltage	At 67%V _{DRM}	115			0.3	V
R _{th(j-h)}	Thermal resistance Junction to heatsink	At 180° sine double side cooled Clamping force 24KN				0.024	°C /W
F _m	Mounting force			19		26	KN
T _{stg}	Stored temperature			-40		140	°C
W _t	Weight				470		g
Outline	KT50cT						

Outline

