USR Semiconductor Co., Ltd

T02-XX00
PHASE CONTROL
THYRISTOR

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T_j(°C)	VALUE			UNIT
				Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz single side cooled, T_{hs}=55°C	125			289	A
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz single side cooled, T_{hs}=80°C	125			200	A
V_{DRM} V_{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	V_{DRM}&V_{RRM} tp=10ms V_{DSM}&V_{RSM}= V_{DRM}&V_{RRM}+100V respectively	125	100		2000	V
I_{DRM} I_{RRM}	Repetitive peak current	at V_{DRM} at V_{RRM}	125			40	mA
I_{TSM}	Surge on-state current	10ms half sine wave V_R=0.6V_{RRM}	125			3.8	KA
I^2T	I^2T for fusing coordination					72	A^2s*10^3
V_{TO}	Threshold voltage		125			0.75	V
r_T	On-state slop resistance					1.22	mΩ
V_{TM}	Peak on-state voltage	I_{TM}=600A	125			2.0	V
dv/dt	Critical rate of rise of off-state voltage	V_{DM}=0.67V_{DRM}	125			500	V/μs
di/dt	Critical rate of rise of on-state current	From 67%V_{DRM} to 1000A, Gate source 1.5A t_r ≤0.5μs Repetitive	125			100	A/μs
I_{rm}	Reverse recovery current	I_{TM}=500A,tp=1000μs, di/dt=-20A/μs, V_r=50V	125			90	A
t_{rr}	Reverse recovery time					10	μs
Q_{rr}	Recovery charge					450	μC
I_{GT}	Gate trigger current	V_A=12V, I_A=1A	25	10		250	mA
V_{GT}	Gate trigger voltage			0.8		2.8	V
I_H	Holding current			10		200	mA
V_{GD}	Non-trigger gate voltage	At 67%V_{DRM}	125			0.3	V
$R_{th(j-h)}$	Thermal resistance Junction to heatsink	At 180° sine' single side cooled Clamping torque 27 N·m				0.15	°C /W
F_m	Mounting torque			25		30	N·m
T_{stg}	Stored temperature			-40		140	°C
Outline							

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