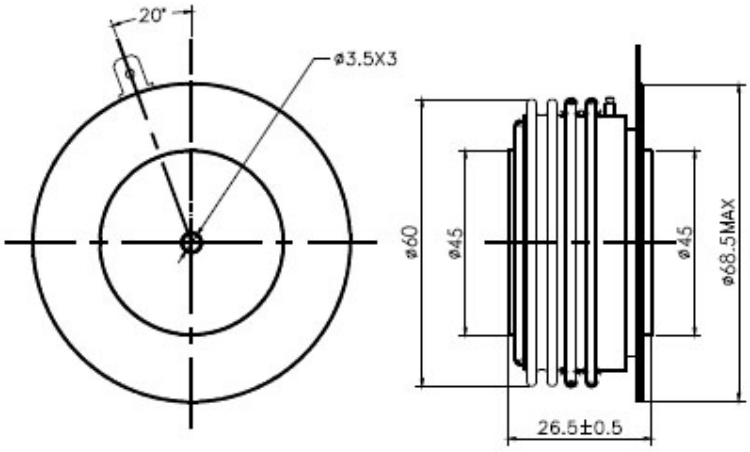
USR Semiconductor Co., Ltd

T04-XX00
PHASE CONTROL
THYRISTOR

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T_j(°C)	VALUE			UNIT
				Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled,T_{hs}=55°C	125			855	A
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled,T_{hs}=80°C	125			646	A
V_{DRM} V_{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	V_{DRM}&V_{RRM} tp=10ms V_{DsM}&V_{RsM}= V_{DRM}&V_{RRM}+100V respectively	125	800		1800	V
I_{DRM} I_{RRM}	Repetitive peak current	at V_{DRM} at V_{RRM}	125			40	mA
I_{TSM}	Surge on-state current	10ms half sine wave V_R=0.6V_{RRM}	125			9.2	KA
I^2T	I^2T for fusing coordination					423	A^2s*10^3
V_{TO}	Threshold voltage		125			0.91	V
r_T	On-state slop resistance					0.68	mΩ
V_{TM}	Peak on-state voltage	I_{TM}=1700A, F=15KN	125			2.07	V
dv/dt	Critical rate of rise of off-state voltage	V_{DM}=0.67V_{DRM}	125			300	V/μs
di/dt	Critical rate of rise of on-state current	From 67%V_{DRM} to 1000A, Gate source 1.5A t_r≤0.5μs Repetitive	125			300	A/μs
I_{rm}	Reverse recovery current	I_{TM}=500A,tp=1000μs, di/dt=-20A/μs, V_r=50V	125			140	A
t_{rr}	Reverse recovery time					15	μs
Q_{rr}	Recovery charge					1050	μC
I_{GT}	Gate trigger current	V_A=12V, I_A=1A	25	35		250	mA
V_{GT}	Gate trigger voltage			0.8		2.5	V
I_H	Holding current			20		200	mA
V_{GD}	Non-trigger gate voltage	At 67%V_{DRM}	125			0.3	V
Rth(j-h)	Thermal resistance Junction to heatsink	At 180° sine double side cooled Clamping force 15KN				0.035	°C /W
F_m	Mounting force			10		20	KN
T_{stg}	Stored temperature			-40		140	°C
W_t	Weight				270		g
Outline	KT33cT						

Outline



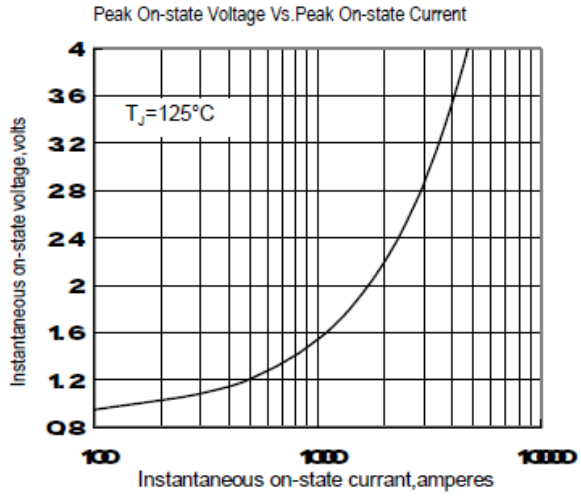


Fig.1

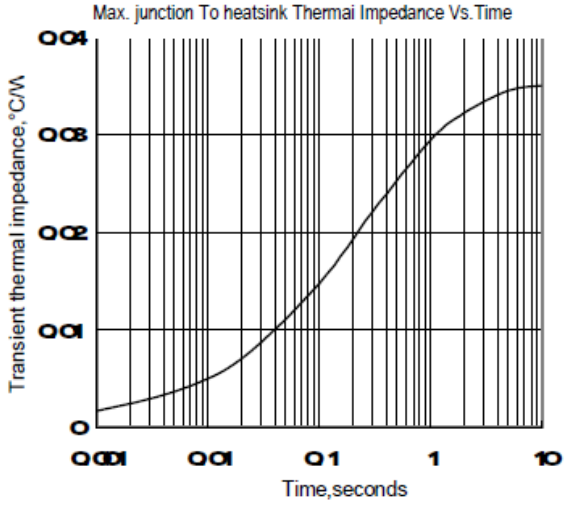


Fig.2

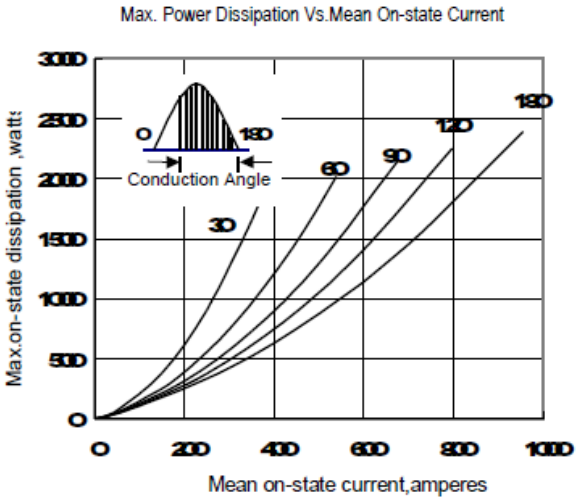


Fig.3

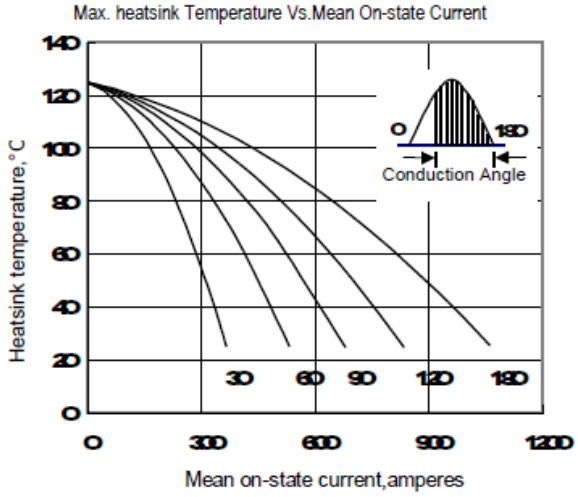


Fig.4

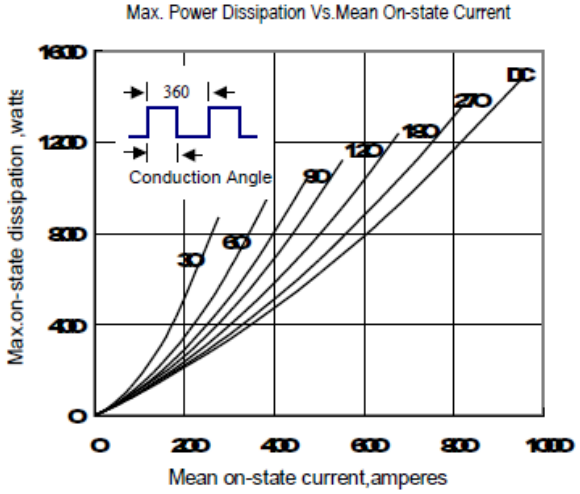


Fig.5

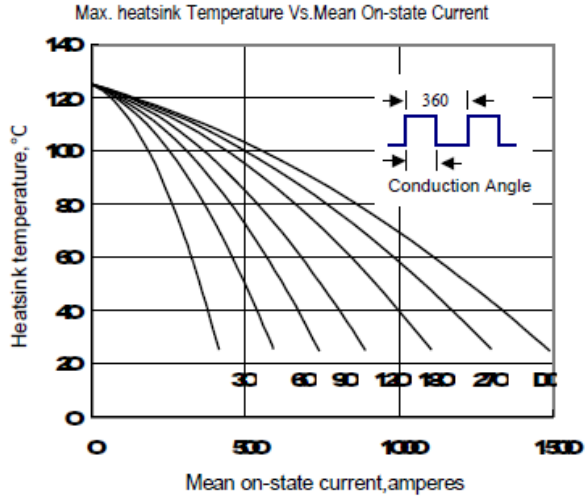


Fig.6

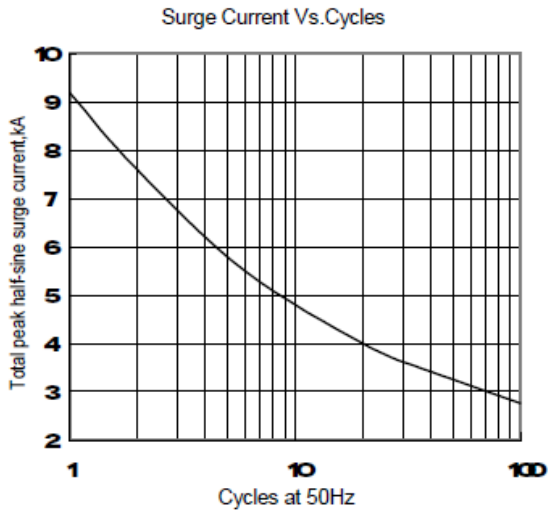


Fig.7

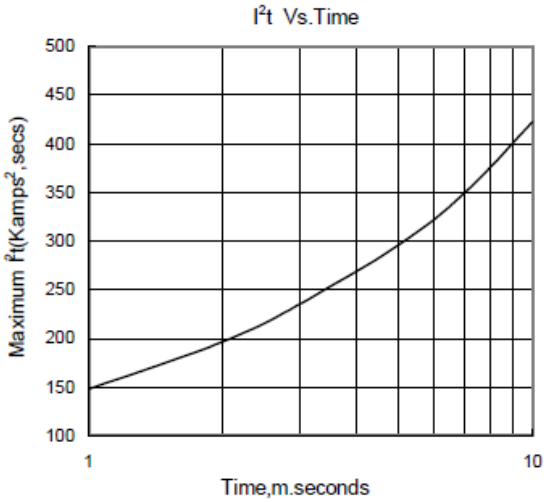


Fig.8

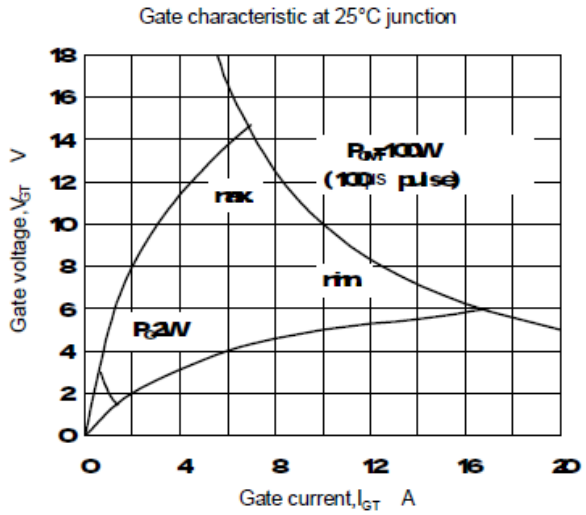


Fig.9

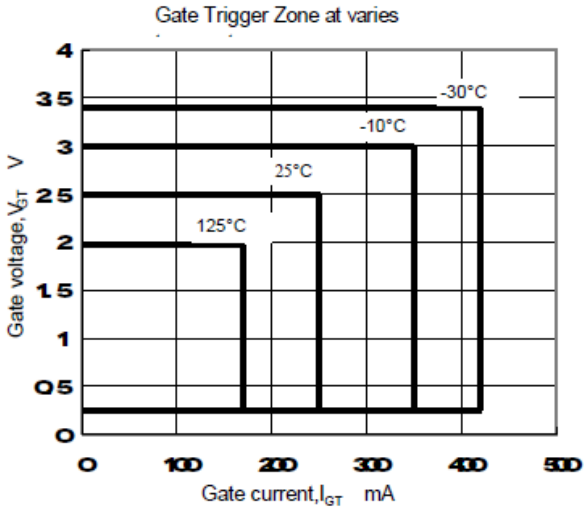


Fig.10