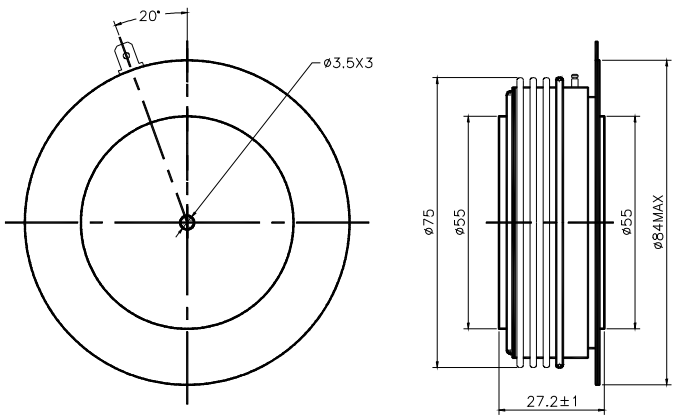
USR Semiconductor Co., Ltd

T12-XX00
PHASE CONTROL
THYRISTOR

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T_j(°C)	VALUE			UNIT
				Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled,T_{hs}=55°C	125			1505	A
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled,T_{hs}=80°C	125			1115	A
V_{DRM} V_{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	V_{DRM}&V_{RRM} tp=10ms V_{DSM}&V_{RSM}= V_{DRM}&V_{RRM}+100V respectively	125	2700		3600	V
I_{DRM} I_{RRM}	Repetitive peak current	at V_{DRM} at V_{RRM}	125			120	mA
I_{TSM}	Surge on-state current	10ms half sine wave V_R=0.6V_{RRM}	125			23	KA
I^2T	I^2T for fusing coordination					2645	A^2s*10^3
V_{TO}	Threshold voltage		125			1.14	V
r_T	On-state slop resistance					0.32	mΩ
V_{TM}	Peak on-state voltage	I_{TM}=3220A, F=28KN	125			2.17	V
dv/dt	Critical rate of rise of off-state voltage	V_{DM}=0.67V_{DRM}	125			500	V/μs
di/dt	Critical rate of rise of on-state current	From 67%V_{DRM} to 1500A, Gate source 1.5A t_r ≤0.5μs Repetitive	125			400	A/μs
I_{rm}	Reverse recovery current	I_{TM}=1000A,tp=1000μs, di/dt=-20A/μs, V_r=50V	125			190	A
t_{rr}	Reverse recovery time					21	μs
Q_{rr}	Recovery charge					1995	μC
I_{GT}	Gate trigger current	V_A=12V, I_A=1A	25	40		300	mA
V_{GT}	Gate trigger voltage			0.8		3.0	V
I_H	Holding current			20		300	mA
V_{GD}	Non-trigger gate voltage	At 67%V_{DRM}	125			0.3	V
$R_{th(j-h)}$	Thermal resistance Junction to heatsink	At 180^0 sine' double side cooled Clamping force 28KN				0.020	°C /W
F_m	Mounting force			21		30	KN
T_{stg}	Stored temperature			-40		140	°C
W_t	Weight				650		g
Outline	KT54cT60						

Outline



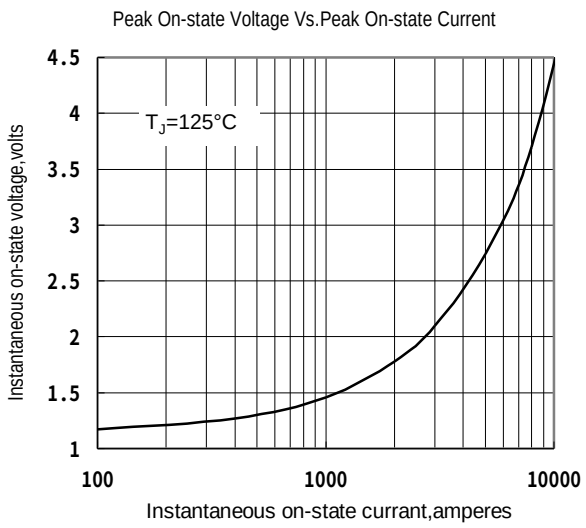


Fig.1

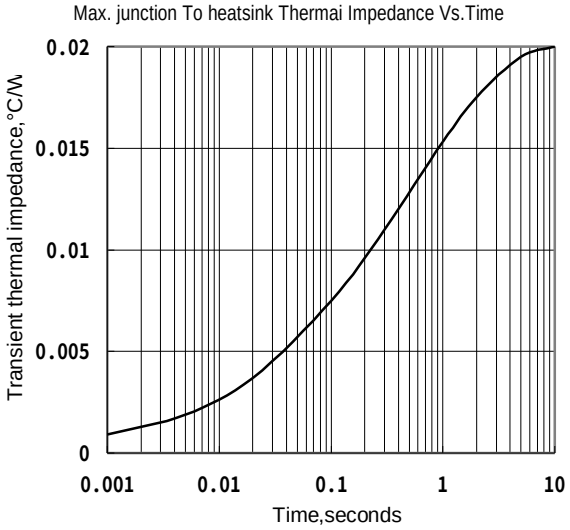


Fig.2

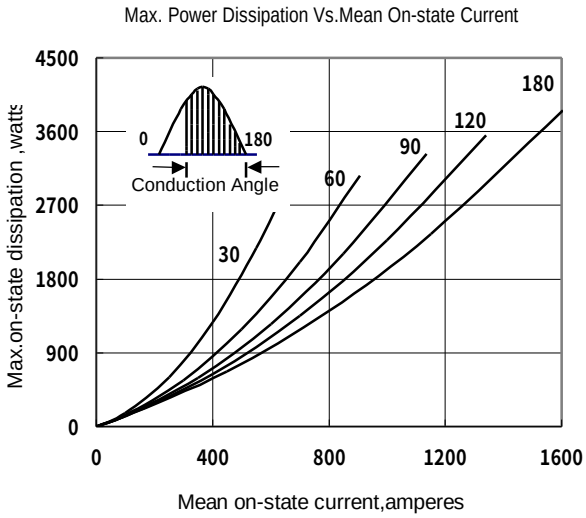


Fig.3

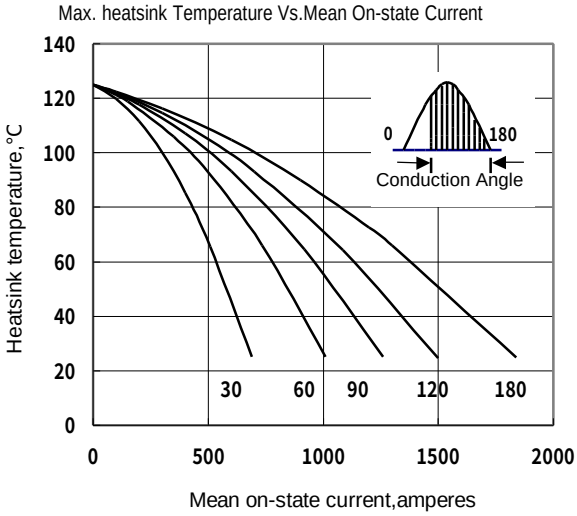


Fig.4

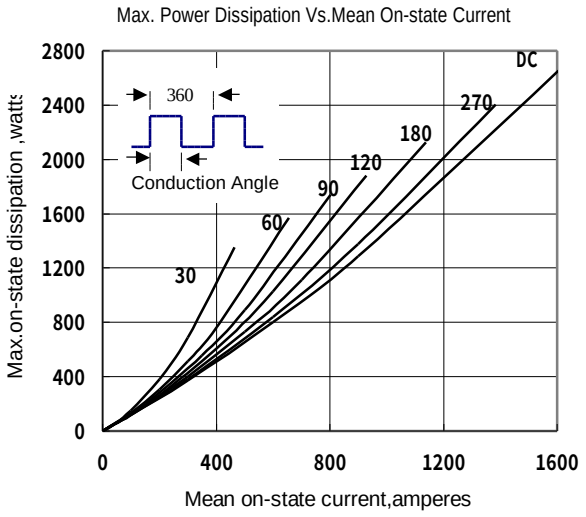


Fig.5

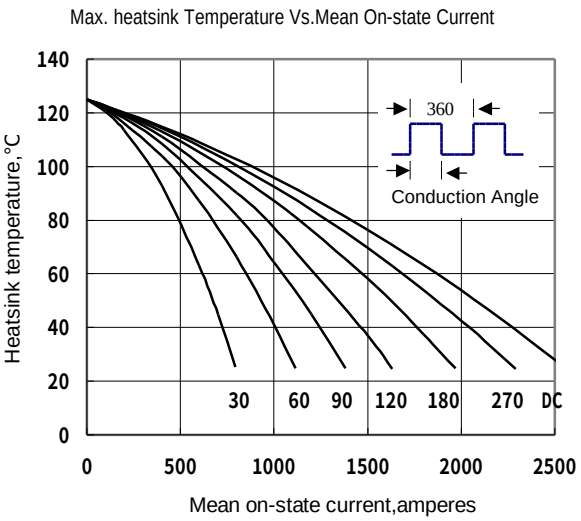


Fig.6

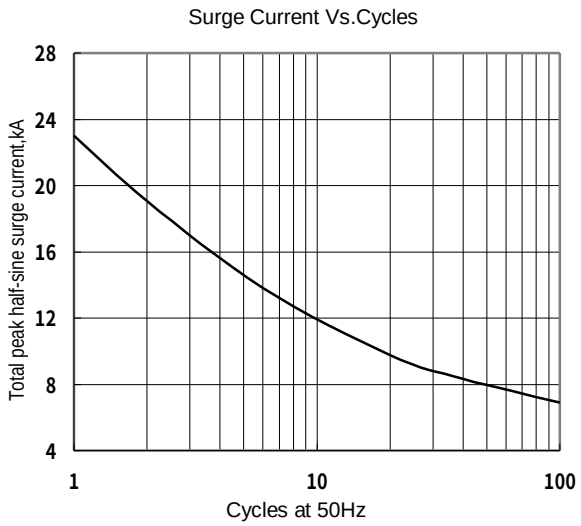


Fig.7

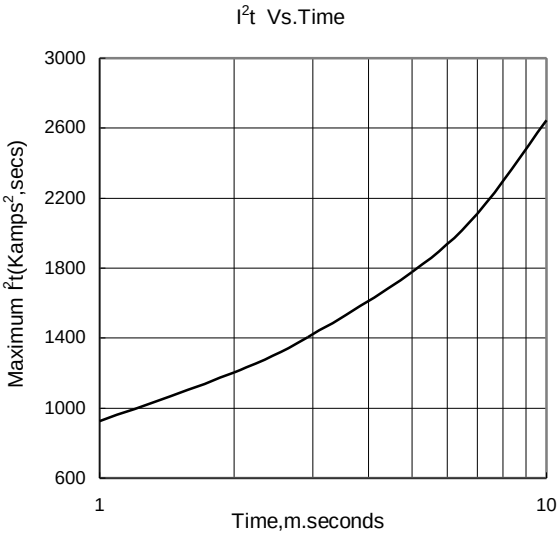


Fig.8

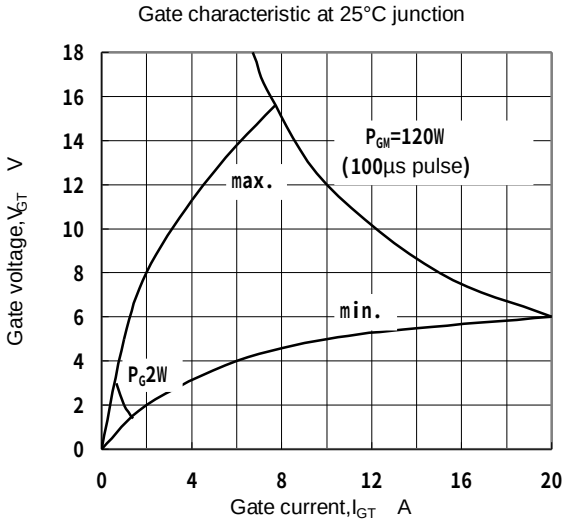


Fig.9

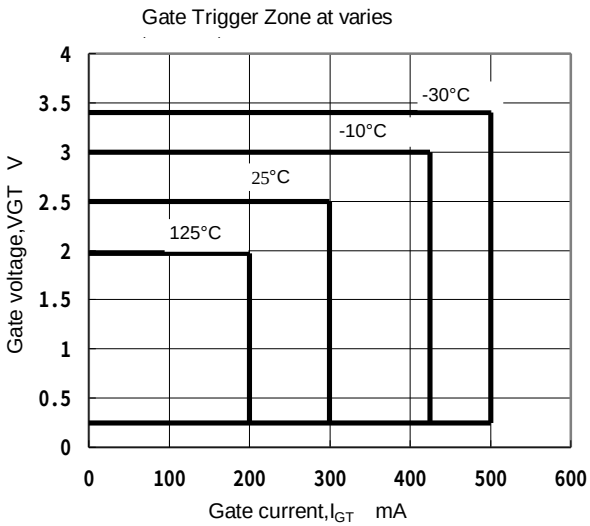


Fig.10